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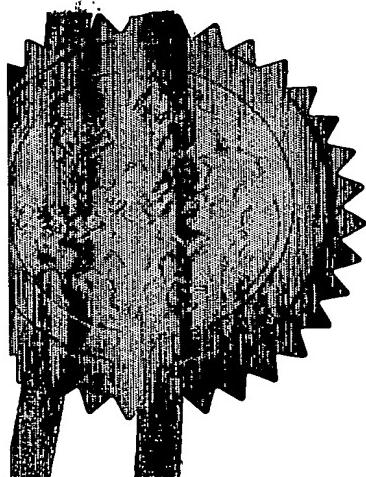
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P3158 GB PRO

- 9 APR 2003

2. Patent application number

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0308180.9

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AOTI OPERATING COMPANY, INC.  
131 NW HAWTHORNE AVENUE  
SUITE 207  
BEND, OREGON 97701, US

Patents ADP number (if you know it)

If the applicant is a corporate body, give the country/state of its incorporation

DELAWARE, USA

8113825002

4. Title of the invention

OVERLAY ALIGNMENT MARK

5. Name of your agent (if you have one)

NOVAGRAAF PATENTS LIMITED

"Address for service" in the United Kingdom to which all correspondence should be sent (including the postcode)

THE CRESCENT  
54 BLOSSOM STREET  
YORK YO24 1AP

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08299166001

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Country

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Number of earlier application

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- a) any applicant named in part 3 is not an inventor, or
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Description 16

Claim(s)

Abstract

Drawing(s) 2 *MW* *6A*

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Statement of inventorship and right to grant of a patent (Patents Form 7/77)

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I/We request the grant of a patent on the basis of this application.

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Date

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12. Name and daytime telephone number of person to contact in the United Kingdom PETER WILSON (DR)

01904 610586

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~~DUPPLICATE~~

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Overlay Alignment Mark

The invention relates to overlay metrology during semiconductor device  
5 fabrication, and in particular to an overlay alignment mark to facilitate  
alignment and/ or measure the alignment error of two layers on a  
semiconductor wafer structure, or different exposures on the same layer,  
during its fabrication.

- 10 Modern semiconductor devices, such as integrated circuits, are typically  
fabricated from wafers of semiconductor material. In particular, a wafer is  
fabricated comprising a succession of patterned layers of semiconductor  
material.
- 15 Overlay metrology in semiconductor device fabrication is used to determine  
how well one printed layer is overlaid on a previously printed layer. Close  
alignment of each layer at all points within the device is crucial for reaching  
the design goals and hence the required quality and performance of the  
manufactured device. It is consequently of importance for the efficiency of  
20 the manufacturing process that any alignment error between two patterned  
layers on a wafer, especially successive patterned layers can be measured  
quickly and accurately. It is similarly important to be able to measure any  
alignment error between successive exposures in the same layer, and where  
reference is made herein for convenience to two layers it will be understood  
25 where appropriate to apply equally to two exposures in the same layer.

Misregistration between layers is referred to as overlay error. Overlay  
metrology tools are used to measure the overlay error. This information may  
be fed into a closed loop system to correct the overlay error.

Current overlay metrology employs optically readable target patterns, printed onto the successive layers of a semiconductor wafer during fabrication. The relative displacement of two successive layers is measured by imaging the patterns at high magnification, digitizing the images, and processing the image data using various known image analysis algorithms to quantify the overlay error.

The pattern of the target mark may be applied to the wafer by any suitable method. In particular, it is often preferred that the mark is printed onto the wafer layers using photolithographic methods. Typically, the same technique is used to apply overlay target marks on each of two wafer layers to be tested to enable alignment information to be measured which is representative of the alignment of the layers. Accuracy of layer alignment should correspond to accuracy of circuit pattern alignment within the fabricated wafer.

15

Current overlay metrology is normally practised by printing targets with rectangular symmetry. For each measurement two targets are printed, one in the current layer and one in a previous layer, or one in association with each pattern in a common layer. The choice of which previous layer to use is determined by process tolerances. The two targets have a nominally common centre, but are printed with different sizes so that they can be differentiated. Normally, but not always, the target printed in the current layer is the smaller of the two targets. An overlay measurement in such a system is the actual measured displacement of the centres of the two targets.

25

Current preferred practice is that the size of the targets is designed such that both can be imaged simultaneously by a bright-field microscope. Imaging considerations determine that the larger of the two targets is typically a 25 $\mu$ m square on the outside. This arrangement permits capture of all of the necessary data for the performance of the measurement from a single image.

Measurements at a rate of one in every two seconds or less are possible using current technology.

The procedure necessarily requires that the target and its image are symmetric,  
5 since otherwise there is no uniquely defined centre point. Without symmetry there is an uncertainty in the measurement, which may be more than can be tolerated. Within that general requirement, optimal sizes and shapes of current designs of targets to be measured are well known. The targets are positioned in the scribe area at the edge of the fabricated circuit.

10 It is generally highly desirable that the measurement targets maintain axial symmetry about the optical axis of the measurement tool, since accurate measurement requires very close control of image aberrations and this can only be achieved in practice for images at or centred about the system axis. In  
15 most prior art systems, measurements are therefore made from the targets by computing a centre line for each different target. The overlay measurement is the difference in the centre lines. Most of the target designs in general use permit measurement of the vertical and horizontal overlay displacement from a single image.

20 Measurement errors must be controlled to a very small amount. Errors known to arise are classified as random errors, characterized by determination of measurement precision; and systematic errors, characterized by tool induced errors, tool-to-tool measurement differences and errors introduced by  
25 asymmetry in the targets being measured. Successful application of overlay metrology to semiconductor process control is generally held to require that, combined, these errors are less than 10% of the process control budget. This measurement error budget is in practice in the range 1 to 5 nm, and will remain so in the foreseeable future.

Measurement precision is easily determined by analysis of the variations of repeated measurements. Different forms of precision may be determined by well known appropriate methods, allowing determination of the static, short-term and long-term components of precision.

5

Determining the contribution of the measurement tool alone to errors is achieved by comparing measurements made with the target in its normal presentation with a measurement made after rotating the target by 180° with respect to the imaging system. Ideally the measurement will simply change sign. The average of the measurements at 0° and 180° is called *Tool Induced Shift* (TIS), as is well known to those skilled in the art, and is widely accepted as a measure of the tool's systematic error contribution. Measurements of TIS differ from tool to tool and with process layer. Subtraction of the estimated TIS error from the measurements allows removal of the TIS error from the measurements, but at the expense of the additional time taken to measure the target twice.

Different tools, even when of the same type, will make slightly different measurements, even after allowing for precision and TIS errors. The magnitude of this error can be determined experimentally by comparing the averages of repeated measurements at 0° and 180° on two or more tools.

The contributions of precision, TIS and tool-to-tool differences are normally combined through a root-sum-square product, or alternative appropriate method, to determine the total measurement uncertainty due to the measurement process. The total measurement uncertainty must be less than 10% of the overall overlay budget for the process if the metrology is to have value. Existing measurement tools and procedures achieve a total uncertainty within that required for current process technologies but insufficient for future requirements.

By contrast, although the contribution of asymmetry in the measurement target itself is widely understood it is not normally determined. It is known that in many cases it can be much larger than the tool contribution to measurement uncertainty. There are two sources of error to be considered:

- 5 1. Imperfection in the manufacture of the target which leads to an uncertainty in its location. An example of this is physical asymmetry of the target, caused perhaps by uneven deposition of a metal film.
- 10 2. Difference in the displacement of the two layers at the measurement target and the genuine overlay of the same layers in the device being manufactured. These can arise from errors in the design and manufacture of the reticles used to create the patterns on the wafer, proximity effects in the printing process and distortion of the films after printing by other process steps.

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These measurement errors represent a practical limitation of the current state of the art which causes severe problems in the application of overlay metrology to semiconductor process control.

- 20 15 Improvements to the first of these problems can sometimes be achieved by fabricating the features in the measured targets from much smaller objects - lines or holes. These smaller features are printed at the design rule for the process, currently in the range 0.1-0.2  $\mu\text{m}$ , and are grouped close together. They are too small to be individually resolved by the optical microscopes used in overlay metrology tools. The small features are grouped into larger shapes in the pattern of traditional overlay targets. The use of small features avoids some of the mechanisms causing imperfections in the shape of the manufactured targets, in part by taking advantage of the optimization of the manufacturing process for objects of this size and shape.
- 25 30

A further problem is introduced by the size of the targets, which are a significant fraction of the space available in the scribe area surrounding the devices being fabricated. It is desired that the size of these areas be reduced, which means that it is also highly desirable that the measurement targets be  
5 made smaller. However, the size of the target cannot be reduced too much, since accurate measurement requires that the measured features are not significantly smaller than the resolution of the microscope system, and achieving good precision requires that as many as possible of such features are visible in the image.

10

It has been shown (Smith, Nigel P.; Goelzer, Gary R.; Hanna, Michael; Troccolo, Patrick M., "*Minimizing overlay measurement errors*", August 1993, Proceedings of SPIE Volume: 1926 Integrated Circuit Metrology, Inspection, and Process Control VII, Editor(s): Postek, Michael T) that space  
15 must be left between the features printed from the two layers else the proximity of one to another causes an error in the measurement. The magnitude of this error depends on the resolution of the imaging microscope system, but must be 5  $\mu\text{m}$  or greater in practical designs if the measurement error is to be contained within practical limits. This proximity effect further  
20 limits the extent to which the size of the targets can be reduced.

However, high speed is one of the key advantages of existing overlay metrology practice, and any process development must not lose this advantage if it is to be viable in production use. This requirement means that uncertainty reduction by the use of repeated measurements is highly undesirable. There is  
25 thus a general desire to develop alternative overlay patterns and/or analysis methods which apply the basic principles of existing metrologies but in a manner that mitigates some or all of these errors to produce an improved fabrication metrology, and in particular a metrology offering improved accuracy without substantial loss of throughput speed. Moreover, it is  
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desirable to use existing imaging tooling, and so desirable to retain the generally square or rectangular mark geometry familiar in the art.

In accordance with the present invention in a first aspect an overlay mark for determining the relative position between two or more layers of a semiconductor structure or between two or more separately generated patterns on a single layer of a semiconductor structure comprises a first mark portion associated with a first layer or pattern as the case may be and a second mark portion associated with a second layer or pattern as the case may be, wherein the first and second mark portions together constitute, when the mark is properly aligned, at least one pair of test zones, each test zone comprising a first mark section formed as part of the first mark portion and a second mark section formed as part of the second mark portion each comprising a plurality of elongate rectangular mark structures in parallel array adjacently disposed to form the said test zone such that the mark structures in each test zone are in alignment in a first direction within the test zone but are substantially at 90° with respect to the mark structures of at least one other test zone in alignment in a second direction, and wherein the test zones making up the or each pair are laterally displaced relative to each other along one of the said directions.

The invention discloses novel target designs that address the disadvantages of the existing technology, in particular offering generally improved measurement performance in relation to the control of errors discussed above without sacrificing advantages in relation to speed of processing and otherwise.

In order to give effective X-Y information, many prior art mark designs which are similarly made up of rectangular test structures divide the mark area into four zones, respectively corresponding to the X and Y directions for each of the reference and overlay markings. Given the symmetry of the optics

commonly used, these are typically disposed around the optic axis of the instrument, in a square array. Such an array has four fold rotational symmetry. However, in such an arrangement the test zones are typically centred off the X-Y mirror axes of the imaging equipment in use. This can give rise to 5 asymmetry errors.

The present invention exploits the realisation that by combining the test sections in this novel way, test zones can be laterally spaced about the optic axis of the imaging equipment, rather than rotationally disposed therearound, 10 so that each test zone can lie on a mirror axis of the imaging equipment in use and reduce this problem.

The preferred square or rectangular symmetry of the test zones can be retained. Accordingly, each test zone preferably has a generally square or 15 rectangular outline shape, the rectangular directions corresponding to the said first and second directions and to the mirror axes of the imaging equipment in use. Generally square test zones are especially to be preferred. The lateral spacing means each pair of zones can be disposed in use to have mirror symmetry about an axis of the imaging apparatus, with the mid point at the 20 optical centre thereof. Preferably, the test zones in a pair are identically sized and shaped. Where more than one pair is present all of the test zones may be identically sized and shaped, or different pairs may be differently sized and shaped. Where more than one zone pair is present, the mid points for each 25 pair are co-located.

25

A particular advantage of the invention is that existing metrology tools may be simply adapted to measurement of the present target designs, avoiding the costs involved in retooling that radically different methods would require.

- Each mark portion is spatially associated with a layer or pattern under test, so that the measured overlay error is representative of the misalignment between the respective layers or patterns. Overlay marks in accordance with the invention are equally suited to measurement of alignment errors between 5 layers, in particular but not limited to consecutive layers, and alignment error between different exposures in the same layer, and where reference is made herein for convenience to two layers it will be understood where appropriate to apply equally to two exposures in the same structural layer. Where the overlay mark is used to aid measurement of alignment between different 10 layers, the first mark portion is laid down upon a first layer, in particular an uppermost layer, and the second mark portion is laid down upon a second layer below the said first layer, such that the test structures of the second layer are detectable through the first layer. The uppermost mark portion serves as an alignment marking, and the lower mark portion as the reference marking.
- 15 In a simplest embodiment of the invention the number of test zones can be reduced to two. The first and second mark sections of the first zone comprise closely adjacent mark structures in parallel array in a common direction, respectively part of the first (or overlay) mark portion and the second (or 20 reference) mark portion. The first and second mark sections of the second zone are similar arrays but disposed at right angles thereto. Only two test zones are needed to give information in both X and Y directions.
- 25 These two test zones are laterally spaced along a line which is parallel to the direction of the test structures in one zone, and perpendicular in the other zone. As a result both test zones can be located generally on an axis of mirror symmetry of the scanning apparatus, which is not possible in conventional overlay marks comprising four test zones in a square array. Improved accuracy in overlay error measurements is offered by this closer association 30 with the axis of symmetry of typical imaging apparatus.

In an alternative embodiment the mark comprises more than one pair of test zones. Each pair is laterally disposed equidistantly about a common centre in one or other of the said two directions. In a particularly preferred embodiment,  
5 a single such pair is disposed in a first direction and a single such pair in a second direction. The first and second mark sections of each zone comprise closely adjacent mark structures in parallel array in a common direction, respectively part of the first (or overlay) mark portion and the second (or reference) mark portion. The first and second mark sections of two zones are  
10 in the first direction and the first and second mark sections of the other two zones in similar arrays but disposed at right angles thereto. This may be achieved either in that a zone in each pair has mark structures oriented in each direction, or in that both zones in a pair have a common orientation perpendicular to that of the other pair.

15

These two test zones in each pair are laterally spaced in respectively an X and Y direction about common centres. In particular they are equidistantly spaced. As a result all test zones can lie about an axis of mirror symmetry of the scanning apparatus, which is not possible in conventional overlay marks  
20 comprising four test zones in a square array. The extra information such a four zone array offers can be retained without losing the possibility of the preferred square or rectangular geometry.

The mark structures comprising each mark section are elongate rectangular structures in parallel array. It will be understood that provided the general elongate rectangular outline for these test structures is maintained, the structures need not be single monolithic rectangular structures. As will be familiar to those skilled in the art, each rectangular test structure may be made up of a series of sub structures. For example, each elongate rectangular test

structure may comprise a row or column as the case may be of smaller constituent test structures, for example a row or column of squares.

Each elongate rectangular test structure and/or each constituent test structure  
5 may comprise sub structures down to design rule limits in the manner which will be familiar to address issues of process induced inaccuracy, as is well known. Suitable arrangements, familiar to those skilled in the art, include parallel arrays of elongate rectangular sub-structures in either direction, arrays of square sub-structures, circles in square or hexagonal array, arrays of holes  
10 within a suitably shaped test structure and any combinations or other like patterns. Sub-structure dimensions are set by design rule limits, being typically for present techniques of the order of 100 to several hundreds of nanometres. However advances in manufacturing processes are likely to further reduce these dimensions in the future.

15

The mark sections each comprise elongate rectangular structures in periodic array. Preferably the period is constant in each mark section. Preferably the period is identical in all mark sections. In a particular preferred configuration, all rectangular test structures in a test zone, and more preferably in the whole mark, have identical widths and spacing. In this way, test structures from the overlay and test structures from the reference in a given test zone are all in alignment when the mark is correctly aligned. In particular, each test structure abuts its neighbour to form in combination therewith a single elongate rectangular mark structure when in correct alignment.

25

Each test zone should preferably have a rectangular, and in particular a generally square outline. Given typical overall mark sizes of 25 µm, each test zone is conveniently around a 10 to 12 µm square.

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- The dimensions of each test structure within each zone and the spacing thereof will be optimally determined by and are therefore preferably set with reference to the resolution limit of the imaging microscope. In one implementation therefore each test structure will have a width of around 0.5 to 2  $\mu\text{m}$ . Spacing 5 between test structures in the array will preferably be between  $\frac{1}{2}$  and two structure widths, and in particular around 1 structure width. This will maximise feature density at the resolution limit of the imaging device. Any specific design embodying the principles of the invention will increase the number of feature transitions when compared with many previous designs.
- 10 Each mark section then comprises several test structures in each direction, preferably at least five, while fitting comfortably into a conventional mark area. The additional image detail provides more information content in the image, providing for an improvement in measurement precision.
- 15 In use with a standard imaging device, the test structures making up each mark portion are to be aligned with the vertical and horizontal grid directions of each array parallel to the X-Y symmetry lines of the imaging device. It has been noted that optimal performance depends on measurement being centred on the optic axis of the imaging device. In use the optic axis of the imaging 20 instruments will be located at a point generally equidistant between each test zone pair along a notional line between the centres thereof.
- 25 The test structures making up the array comprising each mark portion may be laid down by any suitable technique known to those skilled in the art, in particular the photolithographic techniques above described.

The advantages of existing target designs are retained. The measurements are made from a single image so that speed is not compromised. The measurement is made using an optical image, so that existing imaging tools

can be used. Overlay error may be quantified using any suitable known or specifically developed image processing technique.

Thus, in accordance with the present invention in a second aspect a method for providing an overlay mark to determine the relative position between two or more layers of a semiconductor structure or between two or more separately generated patterns on a single layer of a semiconductor structure comprises the steps of:

- laying down a first mark portion in association with a first layer or pattern as the case may be;
- and laying down a second mark portion in association with a second layer or pattern as the case may be;
- the first and second mark portions being so structured as to together constitute, when the mark is properly aligned, at least one pair of test zones, each test zone comprising a first mark section formed as part of the first mark portion and a second mark section formed as part of the second mark portion each comprising a plurality of elongate rectangular mark structures in parallel array adjacently disposed to form the said test zone test zone such that the mark structures in each test zone are in alignment within the test zone, said alignment being in a first direction in half of the test zones and in a second direction substantially at 90° thereto in the other test zones, and wherein the test zones making up the or each pair are laterally displaced relative to each other along one of the said directions.
- Similarly, in accordance with the present invention in a third aspect a method for determining the relative position between two or more layers of a semiconductor structure or between two or more separately generated patterns on a single layer of a semiconductor structure comprises the steps of:
- laying down a first mark portion in association with a first layer or pattern as the case may be, and laying down a second mark portion in association with a

14

second layer or pattern as the case may be, the first and second mark portions being so structured as to together constitute at least one pair of test zones as hereinabove described;

- optically imaging the two test zones in the said first and second directions;
- 5 collecting and digitizing the image;
- numerically analysing the digitized data to obtain a quantified measurement of the misalignment of the first and second mark portions.

- Each mark portion is preferably laid down by a photolithographic process.
- 10 Optical imaging of the mark is preferably carried out using bright field microscopy. Other preferred features of the methods will be understood by analogy with the foregoing.

- The invention will now be described by way of example only with reference to
- 15 Figures 1 to 3 of the accompanying drawings, which are general schematics of a mark in accordance with three embodiments of the invention.

- In each of figures, the mark comprises a first or alignment mark portion on a first layer or associated with a first pattern on a common layer, and a second or
- 20 reference mark portion on a second lower layer or associated with a second lower pattern on a common layer. The first mark portion is represented by lighter grey-shaded structures. The second mark portion, configured to be at least partially visible in conjunction with the first, is represented by darker grey-shaded structures.

- 25
- The invention lies in the arrangement of periodic test structures. The periodic structures and any sub-structures making up the test structures are formed using any suitable processes. Typically these will include lithographic processes that are generally known in the art. Misalignment is measured using
- 30 imaging systems and image analysis techniques, which may be standard

systems and techniques that are generally known in the art or systems and techniques modified to be optimized specific to the marks in accordance with the invention.

- 5 Figure 1 illustrates a top plan view of an alignment mark according to one embodiment of the invention. The mark is shown in the intended configuration that results when the tested layers of a structure are in proper alignment. The mark consists of two mark portions, one on each layer, so serving as overlay and reference.

10

- In figure 1 there are two test zones. Each zone has an overall square shape. The zones are spaced along the dotted line equidistantly about the dot so that each square zone is located mirror-symmetrically on the dotted line. In use this is an X or Y mirror direction of the bright field imaging microscope or 15 other device, with the dot being the optic centre.

- In this implementation, four groups of linear mark structures are shown. The lines in the first two groups are oriented vertically making up the first zone, while the lines in the final two groups are oriented horizontally. The pairs of 20 lines are designed to be printed exactly side by side. The overlay measurement is the relative displacement of one set of lines from the other, which may conveniently be measured using any standard or specially modified technique and analysis.

- 25 To optimise differentiation between reference and overlay the line pitch is arranged to be significantly larger than process tolerance limits for overlay error. The pitch of the lines is also arranged to match the resolution of the imaging microscope. Line pitch is conveniently broadly equal to line width, both being around 1  $\mu\text{m}$  in the illustrated implementation.

Figure 2 illustrates a top plan view of an alignment mark according to one embodiment of the invention. The mark is shown in the intended configuration that results when the tested layers of a structure are in proper  
5 alignment. The mark consists of two mark portions, one on each layer, so serving as overlay and reference.

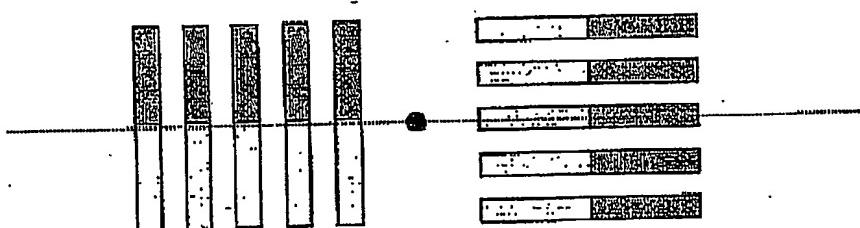
In figure 2 there are four test zones. Each zone has an overall square shape as in figure 1. The zones are identical in size and spaced along the dotted lines  
10 equidistantly in pairs about a common centre. In use these are X and Y mirror directions of the bright field imaging microscope or other device, with the intersection of the lines being the optic centre.

Again each zone consists of an array of lines from the overlay and an array  
15 from the reference. The lines in two of the zones are oriented vertically, while the lines in the final two zones are oriented horizontally. The pairs of lines in each zone are designed to be printed exactly side by side. This produces a cross pattern similar to that of traditional targets, but with each zone symmetrically on the axes whilst retaining a square geometry. This design  
20 meets the goals of separation of the target lines from each layer in order to avoid interaction between the images, axial symmetry and offers more image detail than other designs. The use of isolated groups of lines for each layer also permits application of novel image analysis techniques.

25 Figure 3 illustrates a top plan view of an alignment mark representing a minor variant of figure 2. Again, there are four zones of similar line arrays, but the orientation within equivalent zones is varied. This is intended to illustrate that provided zones are present to give both X and Y measurement, it is not critical  
30 whether the linear structures making up the two zones in each pair share an orientation or are in opposite orientation.

1/2

Figure 1



2/2

Figure 2

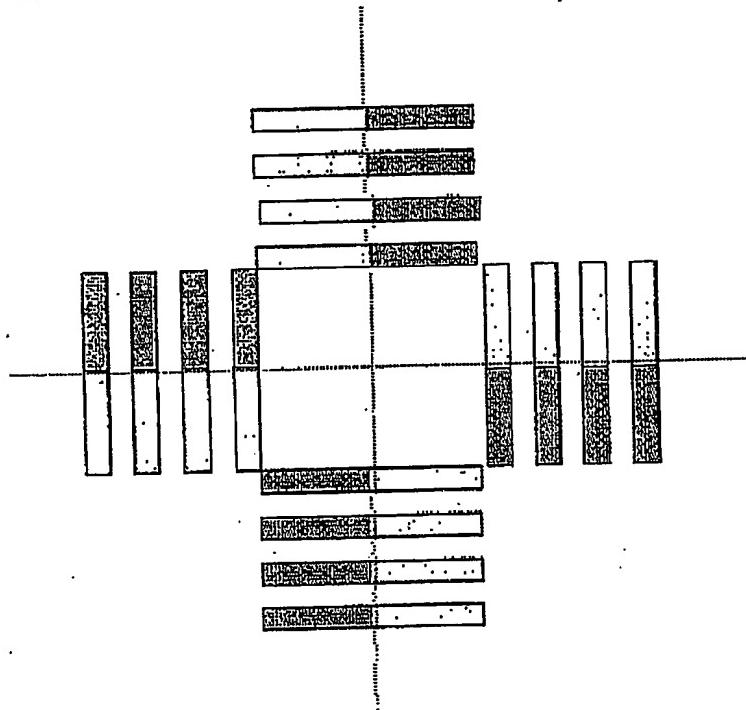
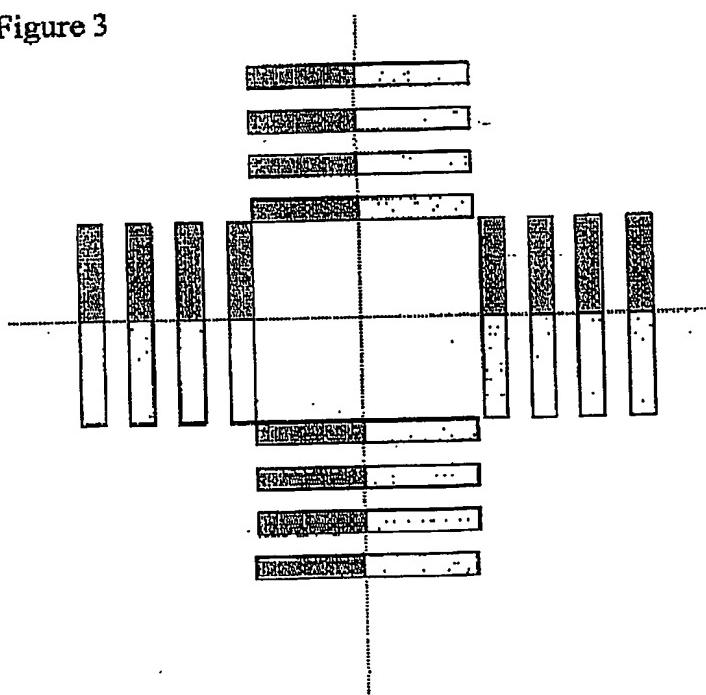


Figure 3



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